

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions,
and listings, of claims in the application:

Listing of Claims:

1-24. (canceled)

25. (currently amended) A system semiconductor device,

comprising:

a system LSI cell portion which includes a plurality of
functional blocks for realizing specific functions, each of the
functional blocks serving as a unit circuit and being arranged on
a semiconductor chip; and

a global wiring layer ~~which at least has~~ comprising a
~~conductor means formed disposed~~ in a substrate and [[a]] at least
~~one wiring layer of a single layer or a multi layer structure~~
~~formed arranged~~ on the conductor, the global wiring layer being
~~means and which is~~ laminated with the system LSI cell portion so
that the functional blocks are electrically connected to each
other;

wherein the conductor in the global wiring layer is a
buried via disposed in the substrate and the at least one wiring
layer comprises first and second wiring layers, the first wiring
layer being disposed on the buried via, an insulating layer being
disposed on the first wiring layer, the second wiring layer being
disposed on the insulating layer and electrically connected to the

first wiring layer through the via, and an adhesive layer being disposed on the insulating layer in an area where the second wiring layer is not positioned.

26. (canceled)

27. (canceled)

28. (currently amended) A system semiconductor device ~~as claimed in claim 25,~~ comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer comprising a conductor disposed in a substrate and at least one wiring layer arranged on the conductor, the global wiring layer being laminated with the system LSI cell portion so that the functional blocks are electrically connected to each other;

wherein the conductor in the global wiring layer ~~has~~ is a secondary wiring layer ~~as the conductor means formed~~ disposed in the substrate, and the substrate is made of an organic material, the at least one wiring layer comprising first and second wiring layers, [[a]] the first wiring layer ~~formed~~ being disposed on the secondary wiring layer, an insulating layer ~~formed~~ being disposed on the first wiring layer, [[a]] the second wiring layer ~~formed~~ being disposed on the insulating layer and

electrically connected to the first wiring layer through a via, and an adhesive layer ~~formed~~ being disposed on the insulating layer in an area where the second wiring layer is not ~~formed~~ positioned.

29. (canceled)

30. (canceled)

31. (currently amended) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a bump which is arranged on a substrate surface on ~~the~~ a side ~~where~~ opposite the wiring layer ~~is not formed~~ and which is adapted to be electrically connected to an external circuit through the conductor ~~means~~.

32. (canceled)

33. (currently amended) A system semiconductor device as claimed in claim 25, wherein the global wiring layer ~~has~~ comprises at least one or more additional said insulating layers ~~as the insulating layer~~.

34. (previously presented) A system semiconductor device as claimed in claim 25, wherein:

a plurality of the system LSI cell portions are formed on a semiconductor wafer;

a plurality of the global wiring layers are formed on the semiconductor substrate; and

the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.

35-46. (canceled)

47. (currently amended) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions and which has pads formed on the functional blocks, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

the global wiring layer comprises[[;]]:

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer,

an adhesive layer disposed on the insulating layer in an area where the second wiring layer is not positioned,

a first via which is formed in the insulating layer and which electrically connects the first wiring layer with the second

wiring layer, and

a second via which is buried in the semiconductor substrate and which is electrically connected to the first wiring layer and which serves as an electrode for an external circuit,

the global wiring layer being laminated with the system LSI portion by electrically connecting the functional blocks with the second wiring layer through the pads so that the functional blocks are electrically connected to the external circuit through the first wiring layer and the second wiring layer.